AIW FAQ

AIW-162 Module Power on Sequence			
Category	AIW	**Date**	2026/4/1
Keyword	AIW-162, WiFi, Broadcom AP6275P		
HW model	ECU-1270		
OS version	Linux kernel 6.12_Release_2602092_v1.1.1		

Category

1. Background & Problem Description

During the PVT (Production Verification Test) phase of the ECU1270 project, the R&D team encountered a high failure rate where 5 out of 8 devices failed to detect the AIW-162 Wi-Fi module.

The primary symptom was a **PCIe Enumeration Failure**—the Linux kernel could not find the PCIe device, and no corresponding logs were present in dmesg log during boot up.

The following figure is the PCIe lines waveform measurement:

Blue: CLKREQ0# (pin 53), Red: PERST0# (pin 52),
Green: WL_REG_ON(3.3V) (pin 56), Yellow: 3.3V(pin 2, 4, 72, 74)

2. Root Cause Analysis & Solution

After debugging with the R&D team, they confirmed the issue is related to an incorrect power-on sequence on WL_REG_ON pin and external pull-up resistor.

The AIW-162 can now be recognized correctly by the host after implementing an appropriate delay for the WL_REG_ON pin and removing the external pull-up resistor. For more details, pleas refer to Chapter 3 Appendix below.

3. Appendix

3.1 Pin Definition

Pin #	AIW-162 Name (AP6475P Name)	I/O	Description
52	PERST0# (PCIE_PREST_L)	I	PCIe host indication to reset the device
53	CLKREQ0# (PCIE_CLKREQ_L)	O	PCIe clock request
54	W_DISABLE2# (BT_REG_ON)	I	Low asserting reset for Bluetooth core (must be connect to CPU'S GPIO)
56	W_DISABLE1# (WL_REG_ON)	I	Low asserting reset for WiFi core (must be connect to CPU'S GPIO)
2, 4, 72, 74	3.3V (VBAT)	I	Main power voltage source input
N/A	N/A (VDDIO)	I	I/O Voltage supply input (this pin is not described in AIW-162 datasheet but vendor’s)

3.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

Voltage rails	Min.	Typ.	Max.	Unit
VBAT	3.0	3.3	3.8	V
VDDIO	1.68	1.8	1.98	V

VBAT current consumption 1200mA (Peak), when VBAT = 3.3V

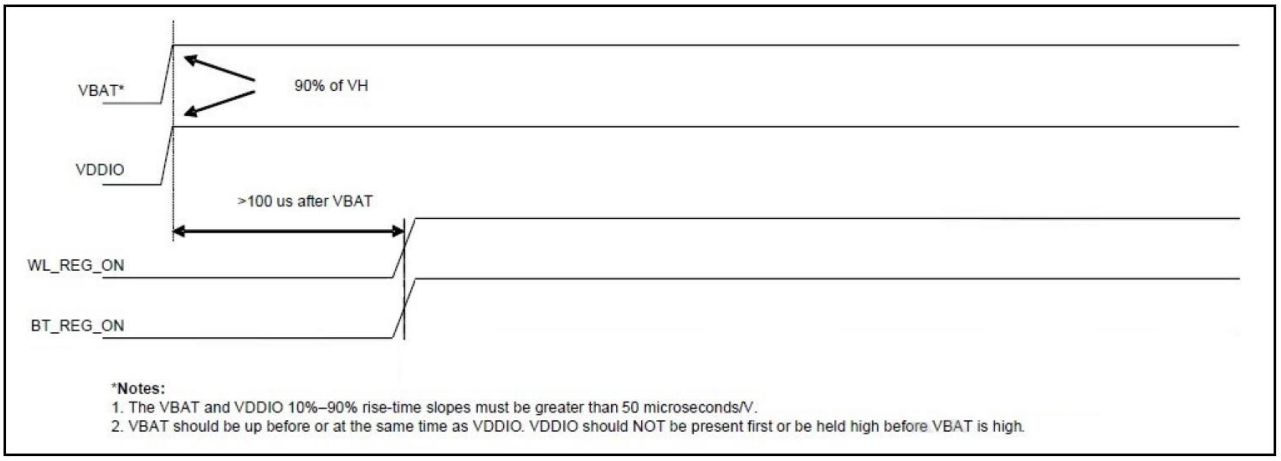
The module requires two power supplies: other Digital I/O Pins.

For VDDIO=1.8V	Min.	Max.	Unit
VIH	0.65×VDDIO	N/A	V
VIL	N/A	0.4xVDDIO	V
VOH output@2mA	VDDIO-0.4	N/A	V
VOL output@2mA	N/A	0.4	V

3.3 Power-up Sequence Timing

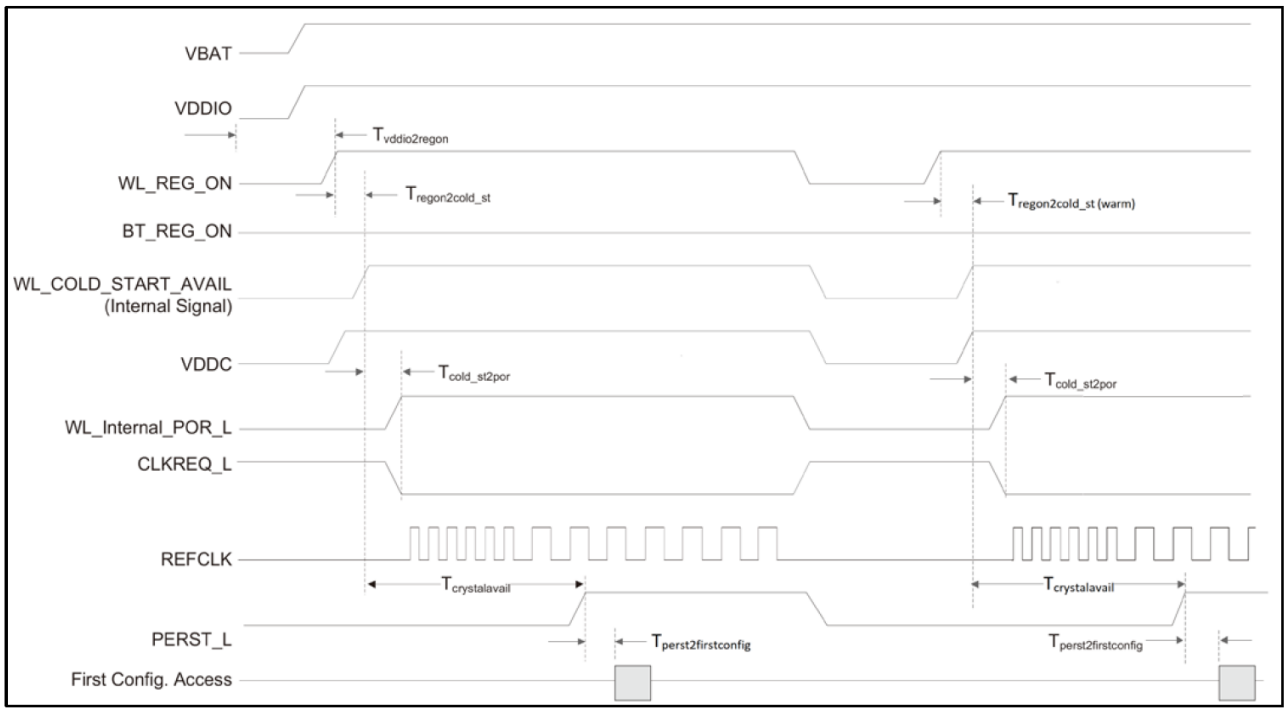
In the following figure, the VDDIO power supply has been included in the module. When VBAT is power-up, VDDIO will rise to high level after 15 ms.

- WL_REG_ON: This signal is used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal regulators.
- It is strongly recommended to connect WL_REG_ON and BT_REG_ON to independent GPIO pins on the CPU. Do not tie them directly to main power rails without delay logic.



WLAN=ON, Bluetooth=ON

3.4 WLAN/PCIe Power-up timing



Timing Parameter	Notes	Value[a]	Unit
$T_{vddio2regon}$	-	0.1	ms
$T_{regon2cold\_st}$	3.4ms+162 instruction-level parallelism	10.13	ms
T_{cold_st2por}	54 ILP cycles	2.24	ms
$T_{crystalavail}$	509 ILP cycles	21.17	ms
$T_{perst2firstconfig}$	-	6.0	ms
$T_{vddioon2firstconfig}$	$T_{vddio2regon}+T_{regon2cold\_st}+T_{crystalavail}+T_{perst2firstconfig}$	37.4[b]	ms
$T_{regon2cold\_st}$ (warm)	162 ILP cycles	6.73	ms

a. The times values assume an ILP tolerance of ±30%

b. With VDDIO as a reference, 37.4 ms is the minimum system wait time before issuing the first configuration access.